Abstracts

GSM 900/DCS 1800 fractional-N frequency synthesizer with very fast settling time

B. Neurauter, G. Marzinger, T. Luftner, R. Weigel, M. Scholz, V. Mutlu and J. Fenk. "GSM 900/DCS 1800 fractional-N frequency synthesizer with very fast settling time." 2001 MTT-S International Microwave Symposium Digest 01.2 (2001 Vol. II [MWSYM]): 705-708 vol.2.

This paper presents a programmable phase-locked-loop (PLL)-based fractional-N frequency synthesizer that uses a third-order /spl Delta//spl Sigma/-modulator. The in-band phase noise of -97 dBc/Hz in the integer-mode and -94 dBc/Hz in the fractional-mode is measured at 30 kHz offset. In addition to offering an ultra-fine frequency resolution of down to 12.4 Hz and very low in-band phase noise this frequency synthesizer offers, with a loop-bandwidth of about 100 kHz, a very fast settling time of less than 95 /spl mu/s when a 75 MHz jump is applied. This feature enables multiple RF applications, including GSM to send a signal and quickly reset to send another signal to meet high data throughput requirements.

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